HMR50N06L

Silicon N-Channel Power MOSFET

General Description :

The HMR50N06L uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications. The package form is TO-252, which accords with the RoHS standard.

Features :

- Fast Switching
- Low Gate Charge and R_{dson}
- Low Reverse transfer capacitances
- 100% Single Pulse avalanche energy Test

Applications :

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

V_{DSS}	60	V
I_D	50	A
P_D	85	W
$R_{DS(ON)type}$	13.5	mΩ

TO-252

Inner Equivalent Principium Chart
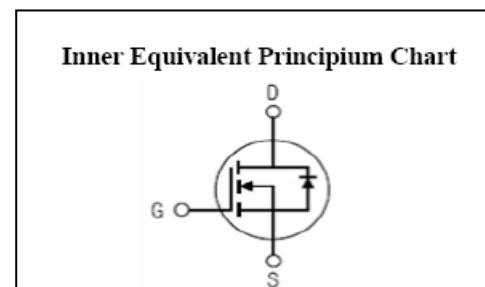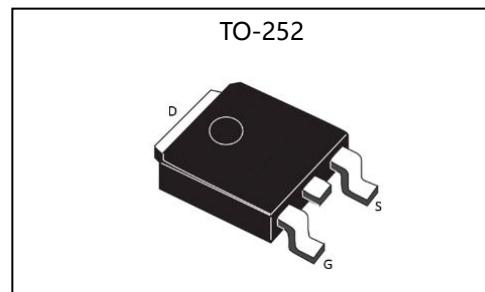
Absolute (Tc= 25℃ unless otherwise specified) :

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	60	V
I_D	Continuous Drain Current	50	A
	Continuous Drain Current T_C = 100 °C	35	A
I_{DM}	Pulsed Drain Current	200	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS} [a2]	Single Pulse Avalanche Energy	300	mJ
E_{AR} [a1]	Avalanche Energy ,Repetitive	50	mJ
I_{AR} [a1]	Avalanche Current	28	A
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	85	W
T_J , T_{stg}	Operating Junction and Storage Temperature Range	175 , −55 to 175	℃
T_L	MaximumTemperature for Soldering	300	℃

Electrical Characteristics (Tc= 25℃ unless otherwise specified)：

OFF Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	$V_{GS}=0V$, $I_D=250\mu A$	60	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	$I_D=250uA$,Reference25℃	--	0.1	--	V/℃
I_{DSS}	Drain to Source Leakage Current	$V_{DS}=60V$,$V_{GS}=0V$,$T_a=25℃$	--	--	1	μA
		$V_{DS}=48V$,$V_{GS}=0V$,$T_a=125℃$	--	--	250	
$I_{GSS(F)}$	Gate to Source Forward Leakage	$V_{GS}=+20V$	--	--	1	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	$V_{GS}=-20V$	--	--	-1	μA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	$V_{GS}=10V$,$I_D=20A$	--	13.5	18	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$,$I_D=250\mu A$	1.5	1.85	2.5	V
Pulse width tp≤380μs,δ≤2%						

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	$V_{DS}=5V$,$I_D=20A$	18	--	--	S
C_{iss}	Input Capacitance	$V_{GS}=0V$,$V_{DS}=30V$ f=1.0MHz	--	2050	--	pF
C_{oss}	Output Capacitance		--	158	--	
C_{rss}	Reverse Transfer Capacitance		--	120	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	$I_D=20A$,$V_{DD}=30V$ $V_{GS}=10V$,$R_G=3.0\Omega$	--	7.5	--	ns
t_r	Rise Time		--	5.0	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	28.0	--	
t_f	Fall Time		--	5.5	--	
Q_g	Total Gate Charge	$I_D=20A$,$V_{DD}=30V$ $V_{GS}=10V$	--	50	--	nC
Q_{gs}	Gate to Source Charge		--	6	--	
Q_{gd}	Gate to Drain（"Miller"）Charge		--	15	--	

Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	50	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	200	A
V_{SD}	Diode Forward Voltage	$I_S=50A, V_{GS}=0V$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$I_S=20A, T_j = 25°C$	--	30	--	ns
Q_{rr}	Reverse Recovery Charge	$dI_F/dt=100A/us, V_{GS}=0V$	--	40	--	nC
Pulse width tp≤380μs,δ≤2%						

Symbol	Parameter	Typ.	Units
$R_{\theta JA}$	Junction-to-Ambient	1.8	°C/W

a1 : Repetitive rating; pulse width limited by maximum junction temperature

a2 : EAS condition : $T_j=25°C$, $V_{DD}=30V, V_G=10V, L=0.5mH, Rg=25Ω$

a3 : $I_{SD} =20A, di/dt ≤100A/us, V_{DD}≤BV_{DS}$, Start $T_J=25°C$

Test Circuit and Waveform
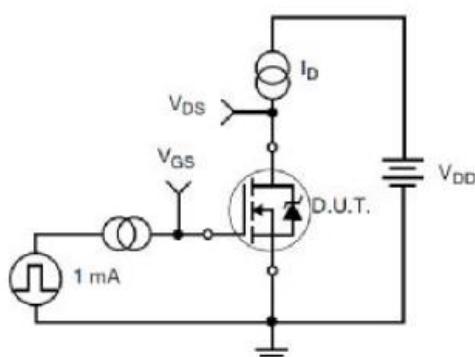
Figure 17. Gate Charge Test Circuit
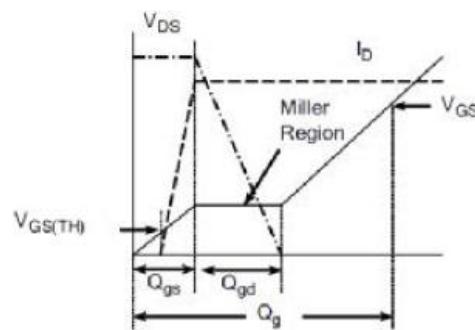
Figure 18. Gate Charge Waveform
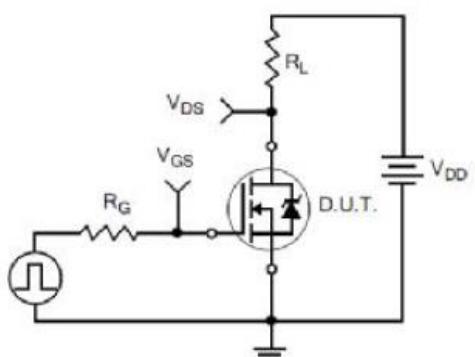
Figure 19. Resistive Switching Test Circuit
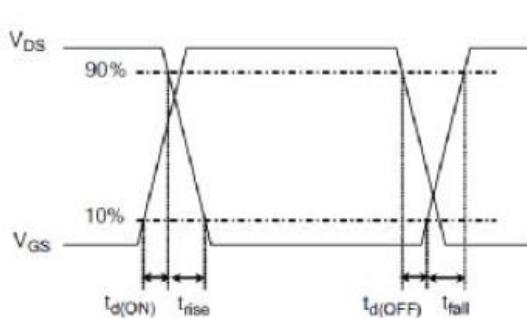
Figure 20. Resistive Switching Waveforms

Characteristics Curve :
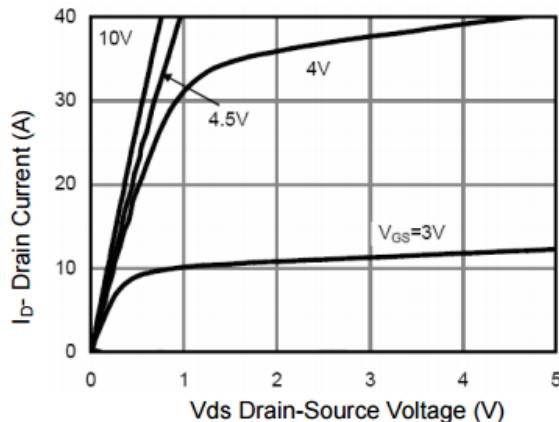
Figure 1 Output Characteristics


Figure 4 Rdson-Junction Temperature

Figure 2 Transfer Characteristics
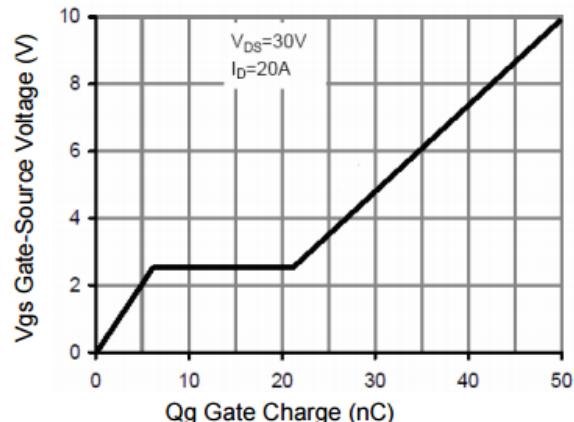
Figure 5 Gate Charge

Figure 3 Rdson- Drain Current
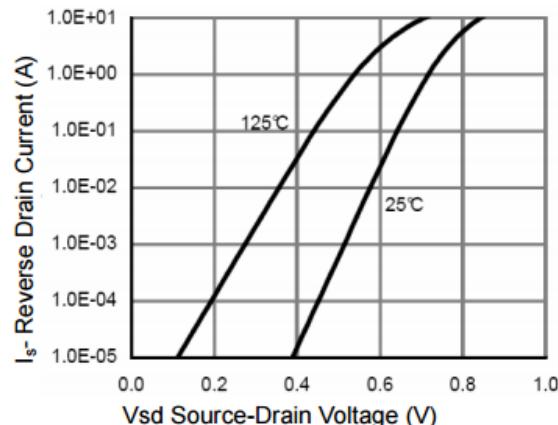

Figure 6 Source- Drain Diode Forward
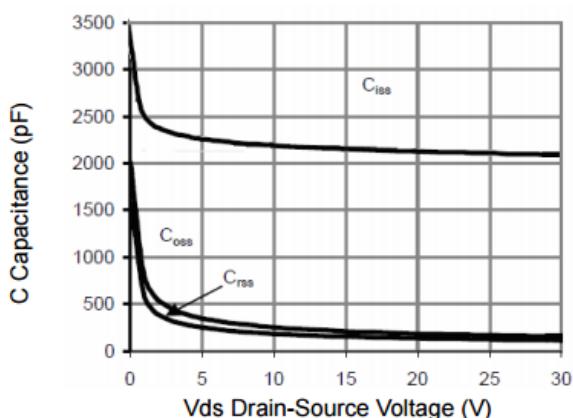
**Figure 7 Capacitance vs Vds**
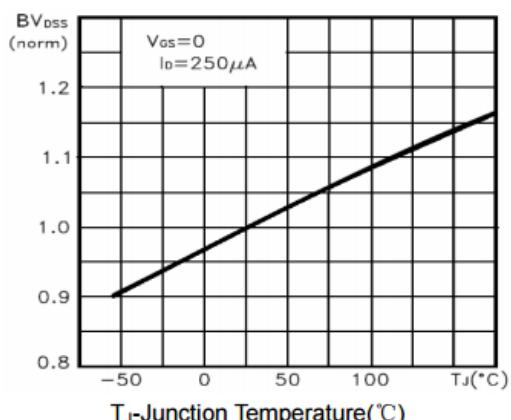
Figure 9 BV$_{DSS}$ vs Junction Temperature
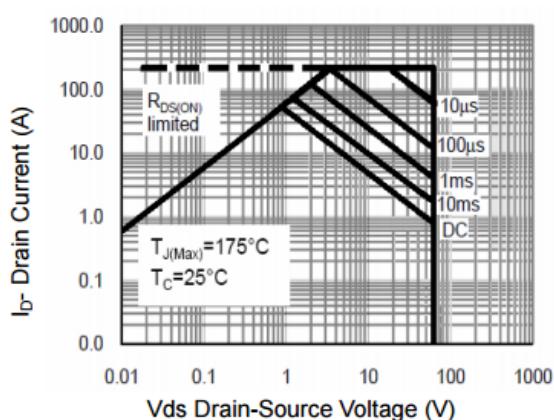
Figure 8 Safe Operation Area
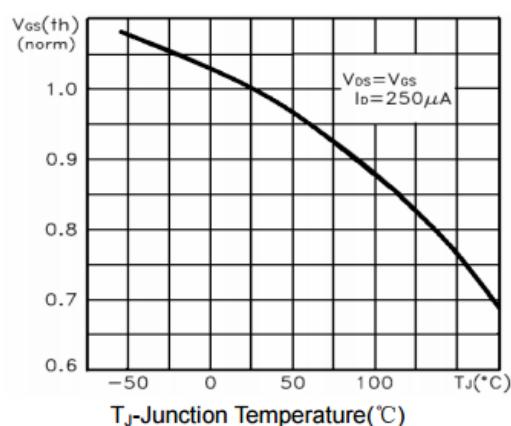
Figure 10 V$_{GS(th)}$ vs Junction Temperature
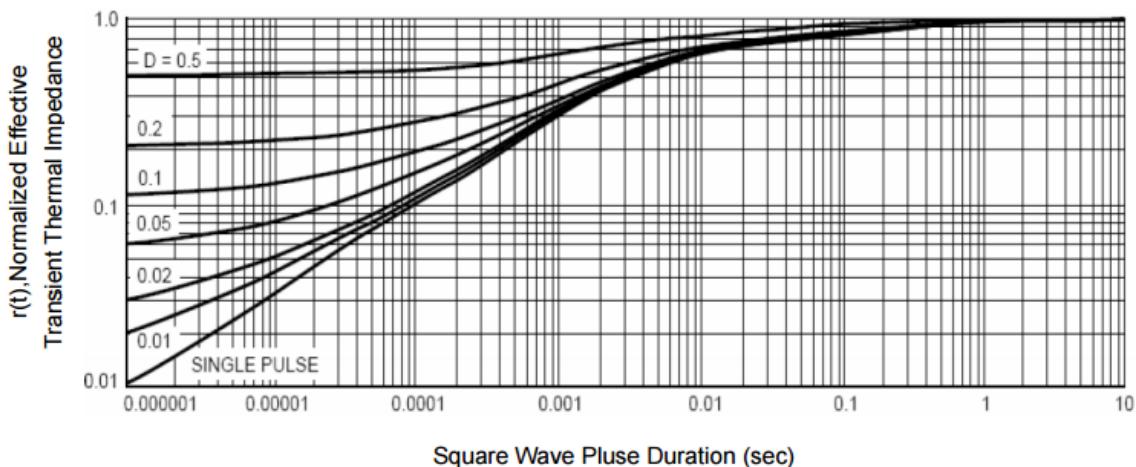
Figure 11 Normalized Maximum Transient Thermal Impedance